

- 25 g) forming a dielectric layer over said substrate; and
26 h) forming a bitline contact to said second bitline
27 region.

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2. The method of claim 1 wherein said second bit line region
60 preferably has an impurity concentration greater than the
cell node region 40 by at least a factor of 10.

3. The method of claim 1 wherein said substrate is doped with
a second conductivity type impurity; second conductivity type
impurity is an n-type impurity; said substrate has an impurity
concentration between $1E17$ and $1E18$ atoms/cc.

4. The method of claim 1 wherein said substrate is p doped and
has a n-well under said word line structure and said
capacitor plate structure, said N-well is doped with a second
conductivity type impurity; second conductivity type impurity
is an n-type impurity; said n-well has an impurity
concentration between $1E17$ and $1E18$ atoms/cc.

5. The method of claim 1 wherein said second bitline region
has a concentration between $1E20$ and $1E21$ atom/cc.

6. The method of claim 1 wherein said first bit line region
has a p-type doping and has an impurity concentration between

1E18 and 1E 19 Atoms/cc, said second bit line region has a p-type doping and has a impurity concentration between 1E20 and 1E21 atoms/cc and said cell node region has a p-type doping and has an impurity concentration between 1E18 and 1E19 atom/cc.

7. The method of claim 1 wherein said first bit line region has a p-type doping and has an impurity concentration between 1E18 and 1E 19 Atoms/cc, said second bit line region has a p-type doping and has a impurity concentration between 1E20 and 1E21 atoms/cc and said cell node region has a p-type doping and has an impurity concentration between 1E17 and 1E18 atom/cc.

8. A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of :

a) forming a word line structure and a capacitor plate structure on a substrate;

(1) a capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor;

- (2) said substrate is p doped and has a n-well under said word line structure and said capacitor plate structure, said N-well is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said n-well has an impurity concentration between $1E17$ and $1E18$ atoms/cc;
- b) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure, said cell node region and said first bit line region do not intersect;
- (1) said first bit line region and said cell node region have a p-type doping and have an impurity concentration between $1E18$ and $1E19$ atoms/cc,
- c) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;
- d) forming a mask pattern over said cell node;
- e) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node; said second bitline region has a concentration between $1E20$ and $1E21$ atom/cc;
- f) removing the mask pattern;

- 38 g) forming a dielectric layer over said substrate; and
39 h) forming a bitline contact to said second bitline
40 region.
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1 9. A structure for a 1T SRAM comprising:

- 2 a) a word line structure and a capacitor plate structure
3 on a substrate; a cell node in said substrate between
4 said word line structure and said capacitor plate
5 structure ; a bit line region in said substrate
6 adjacent to said word line structure, said cell node
7 region and said bit line region do not intersect;
8 b) said capacitor plate structure comprised of a capacitor
9 dielectric on said substrate and a conductive plate
10 layer on said capacitor dielectric; said capacitor plate
11 structure overlying a plate region of said substrate;
12 said plate region and said conductive plate layer acting
13 as one plates of a capacitor;
14 c) said bit line region consists of a first bit line
15 region and a second bit line region; said first bit line
16 region has the same impurity concentration as said cell
17 node; said second bit line region has an impurity

18 concentration greater than said cell node by at least a
19 factor of 10.

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10. The structure of 9 wherein said substrate is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said substrate has an impurity concentration between $1E17$ and $1E18$ atoms/cc.

11. The structure of 9 wherein said substrate is p doped and has a n-well under said word line structure and said capacitor plate structure, said N-well is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said n-well has an impurity concentration between $1E17$ and $1E18$ atoms/cc.

12. The structure of 9 wherein said first bit line region has a p-type doping and has a impurity concentration between $1E18$ and $1E19$ atoms/cc, said second bit line region has a p-type doping and has a impurity concentration between $1E20$ and $1E21$ atoms/cc and said cell node region has a p-type doping and has an impurity concentration between $1E17$ and $1E18$ atoms/cc.

13. The structure of claim 9 wherein said second bit line has an impurity concentration greater than said cell node region by at least a factor of 10.

1 14. A structure for a 1T SRAM comprising:

2 a) a word line structure and a capacitor plate structure
3 on a substrate; a cell node in said substrate between
4 said word line structure and said capacitor plate
5 structure ; a bit line region in said substrate
6 adjacent to said word line structure, said cell node
7 region and said bit line region do not intersect;

8 (1) a capacitor plate structure comprised of a
9 capacitor dielectric on said substrate and a
10 conductive plate layer on said capacitor
11 dielectric; said capacitor plate structure
12 overlying a plate region of said substrate; said
13 plate region and said conductive plate layer acting
14 as plates of a capacitor;

15 (2) said bit line region consists of a first bit line
16 region and a second bit line region; said first bit
17 line region has the same impurity concentration as
18 said cell node; said second bit line region has an
19 impurity concentration greater than said cell node
20 by at least a factor of atoms/cc; said first bit
21 line region has a p-type doping and has a impurity

22 concentration between 1E18 and 1E19 atoms/cc, said
23 second bit line region has a p-type doping and
24 has a impurity concentration between 1E20 and 1E 21
25 atoms/cc, and said cell node region has a p-type
26 doping and has an impurity concentration between
27 1E17 and 1E18 atoms/cc.

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